REMARKS

Claims 1-7, 16-21, 27 and 28 are all the claims pending in the application and elected for prosecution. Claim 1 is amended. Claims 29-32 have been added.

Formal Matters

Applicant notes that the Examiner has not initialed the PTO-1449 form submitted with the Information Disclosure Statement of September 22, 2003 indicating consideration of the non-patent literature documents submitted therewith. Applicant notes that these documents are discussed in paragraph 6 of the specification, and the IDS clearly indicates that the concise statement of relevance is provided by the discussion of the documents in the specification. A copy of the PTO-1449 form is attached for the Examiner's convenience and the Examiner is respectfully requested to initial all of the references on the PTO-1449 indicating that the Examiner has considered those references. Applicant therefore once again kindly requests that the Examiner initial all documents submitted with the IDS and return the initialed PTO-1449 form in the next action.

New claims 29-32 have been added and support for these claims can be found in Figures 6 and 7. Applicant also submits a corrected drawing for Fig. 7 in the form of a replacement drawing. Corrected Fig. 7 now clearly shows the generation of an inversion signal line from a signal line as described in the specification. It is respectfully submitted that no new matter is introduced by the replacement drawing for Fig. 7.

Claim Rejections - 35 U.S.C. § 102

Claims 1, 3 and 27 are rejected under 35 U.S.C. § 102(b) as being anticipated by Kumada et al. (U.S. Application No. 2002/0008686 A1) hereinafter "Kumada".

For at least the following reasons, applicants respectfully traverse the rejections.

Independent Claim 1

Claim 1 is directed to a common drive circuit for a display. Claim 1 recites *inter alia*, a first voltage supply and a second voltage supply which respectively supply a high level voltage signal and a low level voltage signal to a common electrode. Claim 1 also recites at least one signal line is connected to each gate terminal of the first and second transistor, and at least one capacitance load is connected to respective terminals of the first and said second transistors not connected to the first and second voltage supplies. Claim 1 further recites that a high level of a signal passing through the at least one signal line is higher than the high level voltage signal supplied by the first voltage supply and a low level of the signal passing through the signal line is the lower than the low level voltage signal supplied by the second voltage supply. The Examiner contends that Kumada discloses all the features of claim 1.

According to the Examiner, Kumada discloses that Vin (the alleged signal line of claim 1) is either Vdd or GND. See Final Office Action pp. 2-3. Further the Examiner states that Kumada shows in Fig. 3 that the high level voltage signal of claim 1 corresponds to the signal supplied by the positive power source, which Kumada discloses as being equal to Vdd and the low level voltage signal of claim 1 corresponds to the signal supplied by GND, which Kumada discloses as being equal to GND. See Office Action pp 2-3.

Clearly, Vin (alleged signal line of claim 1) is not higher or lower than the signals supplied by the first and second voltage supplies (Vdd and GND) respectively. According to Kumada, Vin can be at most Vdd or GND. Kumada does not teach or suggest that Vin is higher

than Vdd or lower than GND. Accordingly, Kumada does not anticipate claim 1. See [0050] in Kumada.

For the above mentioned reasons, the Examiner is requested to withdraw the rejection.

Dependent Claims 3 and 27

Applicant submits that these claims are allowable at least by virtue of their dependency on the patentable independent claim 1 and by virtue of the features recited therein. Allowance of these claims is therefore requested.

Claim Rejections - 35 U.S.C. § 103

Claims 2, 4-7, 16-21 and 28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kumada et al. (U.S. Application No. 2002/0008686 A1).

For at least the following reasons, applicants respectfully traverse the rejections.

Independent Claim 16

Claim 16 recites a display having a substrate, a display portion integrated on the substrate, a gate driver circuit, and a common drive circuit for the display portion which simultaneously drives capacitance loads in the display portion. Further, claim 16 recites that the common drive circuit is disposed at a position opposite to the gate driver circuit with the display portion between them. The Examiner contends that Kumada teaches the features of claim 16.

The Examiner acknowledges that Kumada does not disclose placing the common drive circuit opposite to the gate driver circuit with the display portion in the middle. However, the Examiner states that such an arrangement is just an obvious matter of design choice and as such does not serve a specific purpose. See Final Office Action page 5.

The Applicant respectfully disagrees. In order to render a claim unpatentable the prior art must teach or suggest all the limitations of the claims. See MPEP 2143.03. The Examiner acknowledges that prior art (Kumada) neither teaches nor suggests placing the common drive circuit opposite to the gate driver circuit, which allows for a symmetrical frame. Further, "The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device", *Ex parte Chicago Rawhide Mfg.* Co., 223 USPW 351, 353 (Bd. Pat. App. & Inter. 1984). Kumada discloses a reference device with a gate driver circuit and a common electrode signal generator circuit. See Fig. 2. However, Kumada does not provide a motivation or reason to modify placement of the above mentioned circuits in the reference device.

Contrary to the allegations in the Office Action, the claimed placement of the gate driver and the common drive circuit is not a mere design choice.

Please refer to Fig. 3 of the present patent application. If the gate driver circuit 3 is disposed on the display substrate 10 next to the display portion 1, it requires a space on the display substrate 10 for the gate driver circuit 3 to be disposed on. On the other hand, it would be desirable to provide another space on the display substrate 10 opposite to the gate driver circuit such that the space allocation is symmetric. Because such a symmetric arrangement would be preferable from a design perspective and for the strength of display portion, the common drive circuit 4 is disposed on the space opposite to the gate driver circuit.

Further, the common driver circuit 4 can be disposed near the input pad to which VCOMH or VCOML is input, or near the power supply circuit which generates VCOMH or

VCOML. By this, it would be possible to reduce the time for reducing the load of the power supply circuit or driving the common electrode. Please refer to page 8 of the specification.

On the other hand, it is described in claim 28 of Kumada (No. US2002/0008686 Al) that the common driver is provided in the source driver. However, the size of the source driver would be large and it makes also the size of the display portion large.

It is required in the industry of mobile communication apparatus that the display apparatus be thin and light, and so the spaces on the display substrate 10 forming a frame around the display portion 1 is required to have a narrow width. It could be realized in the present invention.

Accordingly, the claimed features are not mere design choices. Since Kumada neither teaches nor suggests all of the claimed features, it is respectfully submitted that Kumada does not render claim 16 unpatentable. Therefore, reconsideration and withdrawal of the rejection of claim 16 is requested.

Dependent claims 4 and 19

Claims 4 and 19 recite a common drive circuit comprising pairs of parallel P-type and N-type transistors. The Examiner contends that Kumada teaches the features of claims 4 and 19.

The Examiner cites Fig. 3 in Kumada as teaching all the features of claims 4 and 9. The Examiner further states that C-MOS switches use complementary and symmetrical pairs of p-type and n-type Mosfets for logic functions, such that the MOSFETS are in parallel. See Final Office Action page 7.

Applicant respectfully traverses the rejection. Kumada states that in order to reduce power consumption by the liquid crystal display, the common electrode signal generator circuit

10 as shown in Fig. 3 is composed "only" of a C-MOS switch with no clamp circuit as in the conventional case shown in Fig. 8. See [0049]. Further, Kumada states in [0050] that the arrangement is "extremely simple" and includes "just" a C-MOS switch. Modifying the teachings of Kumada to include pairs of transistors such that the total number of transistors would be more than two would frustrate Kumada's purpose of providing an extremely simple circuit. Therefore, Kumada teaches away from claims 4 and 9. Also, the C-MOS switch shown in Fig. 3 in Kumada is not disclosed to be N-type and P-type transistors in parallel. Further, Kumada does not show an inversion signal line of the input signal. Kumada only shows a control signal Vin (See Fig. 3).

Therefore, applicant submits that claims 4 and 9 are patentably distinguishable from the prior art. The Examiner is requested to reconsider the patentability of claims 4 and 9.

Dependent claim 17

Claim 17 recites *inter alia* features that distinguish over the prior art similar to those features that patentable distinguish claim 1 over the prior art. Claim 17 is thus patentable at least for the reasons claim 1 is patentable. These claims are also patentable by reason of the other limitations contained therein. Further, claim 17 is allowable by virtue of its dependency on independent claim 16.

Dependent Claim 6

Claim 6 recites that the first and second transistors of claim 3 are comprised of thin-film transistors. The Examiner contends that Kumada teaches the features of claim 6.

Applicant respectfully traverses the rejection. Kumada shows that the transistor 6 in Fig. 2 is a thin-film transistor (See Fig. 2 and [0044]). Kumada also states the TFT (thin-film

transistor) 6 is in the liquid crystal panel 1 (See Fig. 2 and [0044]). The transistors shown in Fig. 3 in Kumada are not disclosed as thin-film transistors, as claimed by the Examiner. This is because Fig. 3 in Kumada is a construction of a circuit within a common electrode signal generator 10 (See [0049]). As seen from Fig. 2 in Kumada, the common electrode signal generator 10 is different from the liquid crystal panel 1. Therefore, the transistors of Fig. 3 in Kumada are not disclosed as comprising of thin-film transistors as they are not part of the liquid crystal panel 1.

Therefore, applicant submits that claim 6 is patentable distinguishable from the prior art. The Examiner is requested to reconsider the patentability of claim 6.

Dependent Claim 21

Claim 21 recites *inter alia* features that distinguish over the prior art similar to those features that patentable distinguish claim 6 over the prior art. Claim 21 is thus patentable at least for the reasons claim 6 is patentable. These claims are also patentable by reason of the other limitations contained therein. Further, claim 21 is allowable by virtue of its dependency on independent claim 16.

Dependent Claims 2, 5, and 7

With respect to dependent claims 2, 5, and 7, Applicant submits that these claims are allowable at least by virtue of their dependency and by virtue of the features recited therein. Allowance of these claims is therefore requested.

Dependent Claims 18, 20, and 28

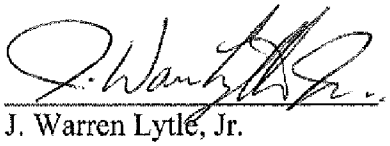
With respect to claims 18, 20, and 28, Applicant submits that these claims are allowable at least by virtue of their dependency and by virtue of the features recited therein. Allowance of these claims is therefore requested.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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